AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions, and listings, of claims in this application.

1. (Currently Amended) A system for designing electronic circuits, comprising:

a memory device for storing a program;

a processor in communication with the memory device, the processor operative with the program to:

receive an original circuit model, wherein the original circuit model has one or more ~~circuit~~ logic gates, wherein each logic gate has a topology;

~~receive a library having one or more logic gates, wherein each logic gate has a topology;~~

calculate current leakage sensitivities for each of the topologies;

provide the current leakage sensitivities to a library; and

synthesize a new circuit model by factoring one or more kernels of the topologies of the original circuit model to determine one or more new topologies having reduced current leakage sensitivities and applying the one or more new topologies to the new circuit model ~~selecting one or more of the topologies based on its leakage sensitivities~~, wherein the new circuit model has a reduced current leakage with respect to the original circuit model.

2. (Original) The system of claim 1, wherein the processor is further operative with the program to:

output the new circuit model.

3. (Currently Amended) The system of claim 1, wherein the current leakage sensitivities are determined by a topology dependent leakage analytical model.

4. (Currently Amended) The system of claim 1, wherein the current leakage sensitivities are determined by measuring the leakage current of the logic gate in a circuit simulator while applying various input patterns to the logic gate.

5. (Currently Amended) The system of claim 1, wherein the processor is further operative with the program when synthesizing to:

optimize current leakage of the new circuit model.

6. (Currently Amended) The system of claim 1, wherein the processor is further operative with the program when synthesizing to:

optimize timing of the new circuit model.

7. (Currently Amended) The system of claim 1, wherein the processor is further operative with the program when synthesizing to:

optimize area of the new circuit model.

8. (Currently Amended) A method for designing electronic circuits, comprising:

receiving an original circuit model, wherein the original circuit model has one or more ~~circuit~~ logic gates, wherein each logic gate has a topology;

~~receiving a library having one or more logic gates, wherein each logic gate has a topology;~~

calculating current leakage sensitivities for each of the topologies;

providing the current leakage sensitivities to a library; and

synthesizing a new circuit model by factoring one or more kernels of the topologies of the original circuit model to determine one or more new topologies having reduced current leakage sensitivities and applying the one or more new topologies to the new circuit model ~~selecting one or more of the topologies based on its leakage sensitivities~~, wherein the new circuit model has a reduced current leakage with respect to the original circuit model.

9. (Original) The method of claim 8, further comprising:

outputting the new circuit model.

10. (Currently Amended) The method of claim 8, further comprising:

receiving a probability model indicating the probability of one or more of the logic gates ~~being~~ in an input state.

11. (Currently Amended) The method of claim 8, further comprising:

receiving a probability model indicating the probability of one or more transistors ~~being~~ in an input state.

12. (Currently Amended) The method of claim 8, wherein the current leakage sensitivities are determined by a topology dependent leakage model.

13. (Original) The method of claim 8, wherein the synthesizing step further comprises:

adding one or more logic gates to the circuit model to create the new circuit model.

14. (Original) The method of claim 8, wherein the synthesizing step further comprises:

deleting one or more logic gates from the circuit model to create the new circuit model.

15. (Original) The method of claim 8, wherein the synthesizing step further comprises:

substituting one or more logic gates from the circuit model to create the new circuit model.

16. (Original) The method of claim 8, wherein the synthesizing step further comprises:

optimizing current leakage of the new circuit model.

17. (Original) The method of claim 8, wherein the synthesizing step further comprises:

optimizing timing of the new circuit model.

18. (Original) The method of claim 8, wherein the synthesizing step further comprises:

optimizing area of the new circuit model.

19. (Currently Amended) The method of claim 8, wherein the logic gates are selected from the group consisting of: and, or, nand, nor, xor, and inverter.

20. (Currently Amended) The method of claim 8, wherein the synthesizing step further comprises:

~~factoring one or more kernels of the circuit model;~~

decomposing one or more portions of the original circuit model into one or more sub-circuits;

mapping one or more circuit gates in one or more of the sub-circuits to one or more of the logic gates in the library that are substituted for the respective circuit gate; and

modifying one or more of the sub-circuits with one or more buffers to create a buffer tree topology.

21. (Original) The method of claim 20, wherein the buffer tree topology comprises buffers having reduced transistor widths.

22. (Original) The method of claim 20, wherein the synthesizing step is performed on sub-circuits that do not have critical timing constraints.

23. (Original) The method of claim 20, wherein the synthesizing step is performed on sub-circuits that have critical timing constraints.

24. (Currently Amended) The method of claim ~~20~~ 8, wherein the factoring step further comprises:

preventing the sharing of logic terms that create excess buffering; and

minimizing total physical area of the circuits on the chip.

25. (Original) The method of claim 20, wherein the mapping step further comprises:

analyzing a tradeoff between gate cloning and buffer insertion.

26. (Original) The method of claim 20, wherein the mapping step further comprises:

analyzing topologies comprising one or more transistor stacks.

27. (Original) The method of claim 20, wherein the mapping step further comprises:

analyzing a leakage tradeoff by considering the probability that one or more of the logic gates is in an input state.

28. (Original) The method of claim 20, wherein the mapping step further comprises:

analyzing a leakage tradeoff by considering the probability that a transistor is in an input state.

29. (Currently Amended) A computer program product comprising a computer useable medium having computer program logic recorded thereon for designing electronic circuits, the computer program logic comprising:

program code for receiving an original circuit model, wherein the original circuit model has one or more ~~circuit~~ logic gates, wherein each logic gate has a topology;

~~program code for receiving a library having one or more logic gates, wherein each logic gate has a topology;~~

program code for calculating current leakage sensitivities for each of the topologies;

program code for providing the current leakage sensitivities to a library; and

program code for synthesizing a new circuit model by factoring one or more kernels of the topologies of the original circuit model to determine one or more new topologies having reduced current leakage sensitivities and applying the one or more new topologies to the new circuit model ~~selecting one or more of the topologies based on its leakage sensitivities~~, wherein the new circuit model has a reduced current leakage with respect to the original circuit model.

30. (Original) The computer program product of claim 29, further comprising:

program code for outputting the new circuit model.

31. (Original) The computer program product of claim 29, further comprising:

program code for optimizing current leakage of the new circuit model.

32-37. (Canceled)

38. (Currently Amended) A system for topology selection to minimize leakage power during synthesis, comprising:

a memory device for storing a program;

a processor in communication with the memory device, the processor operative with the program to:

receive an original circuit design; and

synthesize a new circuit design having a minimized leakage power, wherein the power of the new circuit is minimized by applying ~~an~~ current leakage, area or timing optimization algorithm that incorporates current leakage sensitivities of device topologies, wherein the current leakage optimization algorithm factors one or more kernels of the device topologies of the original circuit design to determine one or more new device topologies having reduced current leakage sensitivities and applies the one or more new device topologies to the new circuit design.

39. (Currently Amended) The system of claim 38, wherein the optimization algorithm is selected from the group consisting of: ~~kernel factoring,~~ decomposition, technology mapping and buffering.

40. (Currently Amended) The system of claim 38, wherein the device topologies are selected from the group consisting of: and, or, nand, nor, xor, and inverter.